Q. P. Code: 10416

Time: 3 Hours **Marks: 80**

N.B : (1) Question No.1 is compulsory.

(2) Attempt any three questions from remaining questions.

(3) Figures to the right indicate full marks.

Q1(a)Multiply using Booth's algorithm (-7) * (3). 5

(b) Explain parallel processing. 5

(c) Write a note on IA-32 register model. 5

(d) Compare Horizontal and Vertical organization. 5

Q2(a)What is cache coherency? Explain various methods to achieve it. 10

(b) Explain microprogramming. Draw and explain microprogrammed control unit. 10

Q3.(a) Consider a 4-way set associative Cache Mapping with Cache Block Size=16 bytes Cache size=8k,Main Memory Size =64k. Design a cache structure and show how the Processor address is interpreted. 10

(b)Why is page replacement algorithm required. Explain how pages are replaced between cache and main memory using replacement policies. 10

Q4 (a) Explain various access methods for I/O devices. 10

(b)Explain how a virtual address is converted into physical address using paging .Also explain Translation Look- aside Buffer. 10

Q5 (a)Explain with examples different addressing modes of IA-32. 10

(b)Write microinstructions for the instruction Add R_0 , $[R_3]$. 5

(c)Explain in brief about Nanoprogramming. 5

Q6(a)Write a note on Flynn's classification. 10

(b) Explain the Hazards in Pipelining and solutions to overcome them. 10

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